What is claimed is:

1. A semiconductor wafer comprising:

a transmitter circuit to output a plurality of substantially constant signal levels;

a receiver circuit to receive the plurality of substantially constant signal levels; and

a control mechanism coupled to the receiver, the control mechanism to calibrate the receiver.

2. The semiconductor wafer of claim 1 further including an integrated circuit die wherein the transmitter circuit and receiver circuit are on the integrated circuit die.

3. The semiconductor wafer of claim 2 further including at least one signal trace coupled between an output of the transmitter circuit and an input of the receiver circuit.

4. The semiconductor wafer of claim 3 wherein the at least one signal trace is at least partially off the integrated circuit die.

5. The semiconductor wafer of claim 3 further including a loopback circuit at least partially off the integrated circuit die.

6. The semiconductor wafer of claim 5 wherein the at least one signal trace comprises a first signal trace coupled between the output of the transmitter circuit and the loopback circuit.

7. The semiconductor wafer of claim 6 wherein the at least one signal trace comprises a second signal trace coupled between the loopback circuit and the input of the receiver circuit.

8. The semiconductor wafer of claim 1 wherein the transmitter circuit includes a pre-emphasis circuit.

9. The semiconductor wafer of claim 1 wherein the receiver circuit comprises a variable offset comparator.

10. The semiconductor wafer of claim 1 wherein the receiver circuit comprises a plurality of variable offset comparators coupled in parallel.

11. An integrated circuit comprising:

a transmitter circuit having a pre-emphasis circuit, the transmitter circuit being coupled to drive an output signal off the integrated circuit;

a receiver circuit coupled to receive an input signal from off the integrated circuit, the receiver circuit including a variable offset comparator; and

a loopback circuit to conditionally couple an output node of the transmitter circuit to an input node of the receiver circuit.

12. The integrated circuit of claim 11 further comprising a control mechanism to influence operation of the transmitter circuit, receiver circuit, and loopback circuit.

13. The integrated circuit of claim 12 wherein the control mechanism comprises a processor.

14. The integrated circuit of claim 12 wherein the control mechanism comprises a state machine.

15. The integrated circuit of claim 12 wherein the control mechanism is adapted to cause the transmitter circuit to output substantially constant amplitude signals using the pre-emphasis circuit.

16. The integrated circuit of claim 11 wherein the receiver circuit comprises a plurality of variable offset comparators coupled in parallel.

17. A method comprising:
transmitting a signal from a transmitter having a pre-emphasis circuit;
receiving the signal at a variable offset comparator; and
calibrating the variable offset comparator.

18. The method of claim 17 wherein calibrating comprises:
sweeping an offset code; and
detecting an output change of state of the variable offset comparator.

19. The method of claim 17 wherein transmitting comprises setting the pre-emphasis circuit to provide a signal having a substantially constant voltage level.

20. The method of claim 17 further comprising repeating the listed actions for a plurality of pre-emphasis circuit settings.

21. The method of claim 20 wherein calibrating comprises:
determining a plurality of offset codes at which the variable offset comparator changes state for the plurality of pre-emphasis circuit settings; and
interpolating between the plurality of offset codes.

22. The method of claim 17 wherein transmitting comprises transmitting from an integrated circuit die, and receiving comprises receiving on the same integrated circuit die.

23. The method of claim 22 wherein the method is performed as part of a wafer level test.

24. The method of claim 17 wherein transmitting comprises transmitting from a first integrated circuit die and receiving comprises receiving at a second integrated circuit die.

25. The method of claim 24 wherein the method is performed as part of a system test.

26. An electronic system comprising:

a first integrated circuit having a transmitter circuit;

a second integrated circuit having a variable offset comparator circuit coupled to the transmitter circuit of the first integrated circuit, and having a control circuit to calibrate the variable offset comparator circuit in response to a signal sent from the transmitter circuit; and

an antenna coupled to first integrated circuit.

27. The electronic system of claim 26 wherein the transmitter circuit includes a pre-emphasis circuit.

28. The electronic system of claim 26 wherein the second integrated circuit includes a plurality of variable offset comparators coupled in parallel.

29. The electronic system of claim 26 wherein the first integrated circuit includes a radio frequency receiver coupled to the antenna.

30. The electronic system of claim 26 wherein the first integrated circuit includes a radio frequency transmitter coupled to the antenna.